



PIN Connection TO-251(I-PAK)

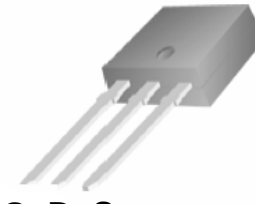
General Description

FIR4N60LG is an N-channel enhancement mode power MOS field effect transistor which is produced using proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC DC converters and H-bridge PWM motor drivers.

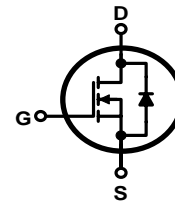
Features

- 4A,600V,  $R_{DS(on)}(typ) = 2.1\Omega @ V_{GS}=10V$
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

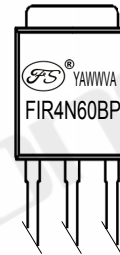


G D S

Schematic diagram



Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- VA = Version & Assembly plant
- FIR4N60BP = Specific Device Code

Absolute Maximum Ratings (Ta = 25°C unless otherwise noted; reference only )

Characteristics	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	±30	V
Drain Current	$I_D$	$T_C=25^\circ C$	4.0
		$T_C=100^\circ C$	2.5
Drain Current Pulsed	$I_{DM}$	16	A
Power Dissipation( $T_C=25^\circ C$ ) -Derate above 25°C	$P_D$	33	W
		0.26	W/°C
Single Pulsed Avalanche Energy(Note 1)	$E_{AS}$	200	mJ
Operation Junction Temperature Range	$T_J$	-55~+150	°C
Storage Temperature Range	$T_{stg}$	-55~+150	°C

**Thermal Characteristics**

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.78	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	110	$^{\circ}\text{C/W}$

**Electrical Characteristics (Ta = 25°C unless otherwise noted; reference only)**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$B_{VDSS}$	25 °C, $V_{GS}=0V$ , $I_D=250\mu A$	600	--	--	V
		125 °C, $V_{GS}=0V$ , $I_D=250\mu A$	600	--	--	V
Drain-Source Leakage Current	$I_{DSS}$	25 °C, $V_{DS}=800V$ , $V_{GS}=0V$	--	--	1	$\mu A$
		125 °C, $V_{DS}=800V$ , $V_{GS}=0V$	--	--	50	$\mu A$
		150 °C, $V_{DS}=800V$ , $V_{GS}=0V$	--	--	100	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 30V$ , $V_{DS}=0V$	--	--	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$ , $I_D=250\mu A$	2.5	--	3.8	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V$ , $I_D=2A$	--	2.1	2.5	$\Omega$
Input Capacitance	$C_{iss}$	$V_{DS}=25V$ , $V_{GS}=0V$ , $f=1.0\text{MHz}$	--	509.00	--	pF
Output Capacitance	$C_{oss}$		--	57.57	--	
Reverse Transfer Capacitance	$C_{rss}$		--	2.59	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=300V$ , $I_D=4A$ , $R_G=25\Omega$  (Note2,3)	--	14.20	--	ns
Turn-on Rise Time	$t_r$		--	27.73	--	
Turn-off Delay Time	$t_{d(off)}$		--	34.67	--	
Turn-off Fall Time	$t_f$		--	28.53	--	
Total Gate Charge	$Q_g$	$V_{DS}=480V$ , $I_D=4A$ , $V_{GS}=10V$  (Note 2,3)	--	11.88	--	nC
Gate-Source Charge	$Q_{gs}$		--	3.33	--	
Gate-Drain Charge	$Q_{gd}$		--	4.90	--	

**Source-Drain Diode Ratings And Characteristics**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse P-N Junction Diode in the MOSFET	--	--	4.0	A
Pulsed Source Current	$I_{SM}$		--	--	16	
Diode Forward Voltage	$V_{SD}$	$I_S=4.0A$ , $V_{GS}=0V$	--	--	1.2	V
Reverse Recovery Time	$T_{rr}$	$I_S=4.0A$ , $V_{GS}=0V$ , $di_F/dt=100A/\mu s$ (Note 2)	--	408	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	1.98	--	$\mu C$

**Notes:**

1.  $L=30\text{mH}$ ,  $I_{AS}=3.45A$ ,  $V_{DD}=100V$ ,  $R_G=25\Omega$ , starting  $T_J=25^{\circ}\text{C}$ ;
2. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ ;
3. Essentially independent of operating temperature.



### Typical Characteristics

Figure 1. On-Region Characteristics

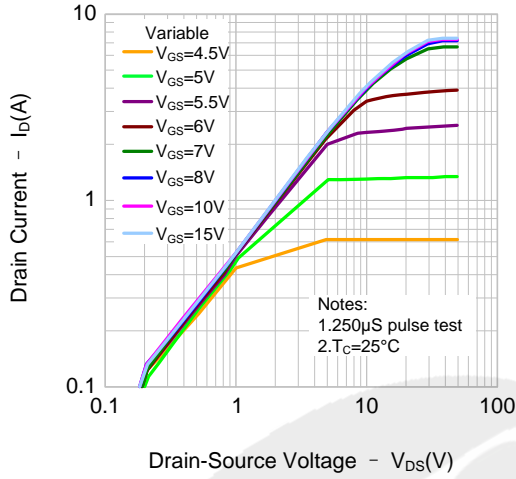


Figure 2. Transfer Characteristics

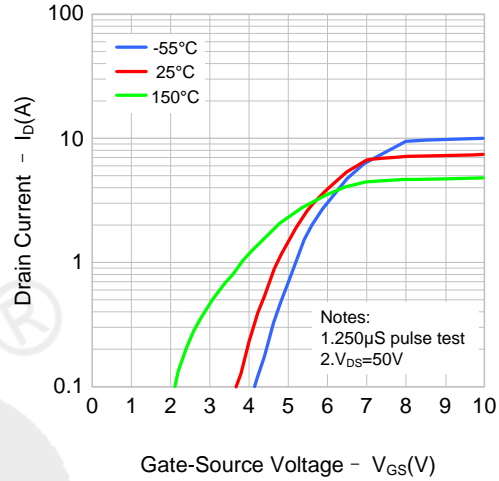


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

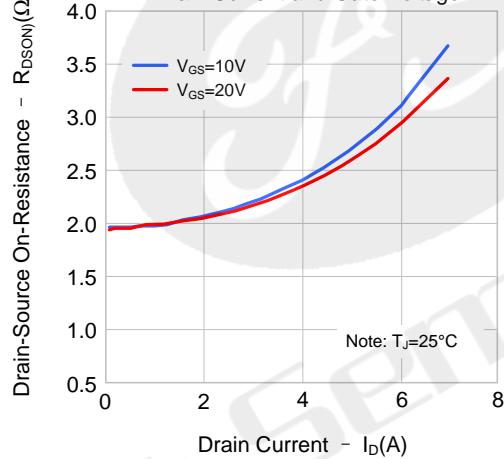


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

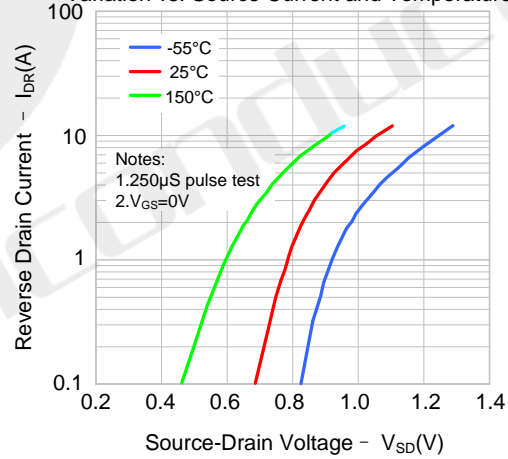


Figure 5. Capacitance Characteristics

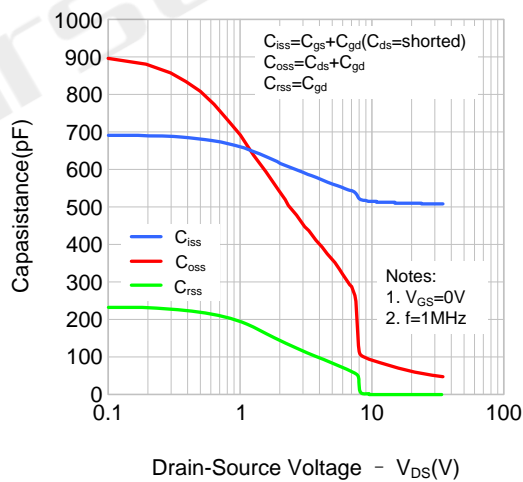
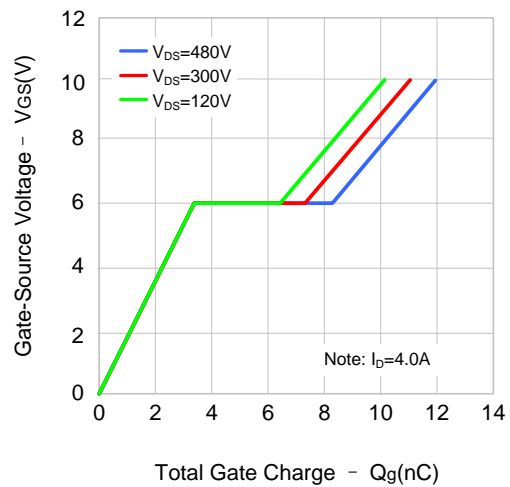


Figure 6. Gate Charge Characteristics





### Typical Characteristics(Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

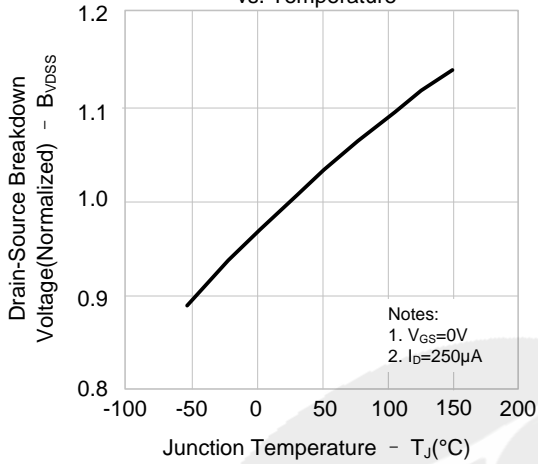


Figure 8. On-resistance Variation vs. Temperature

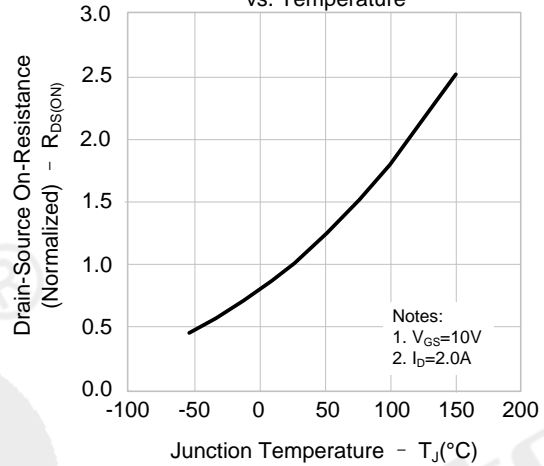


Figure 9. Max. Safe Operating Area(FIR4N60FG)

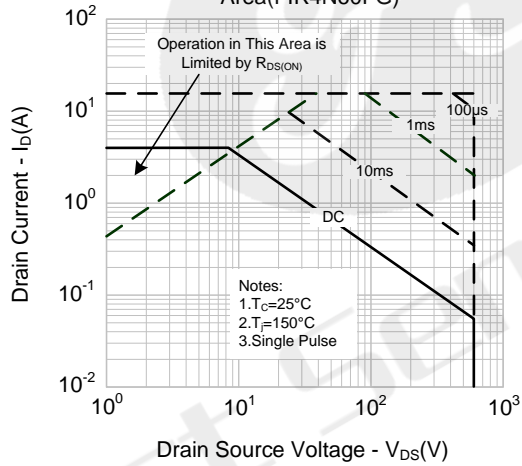
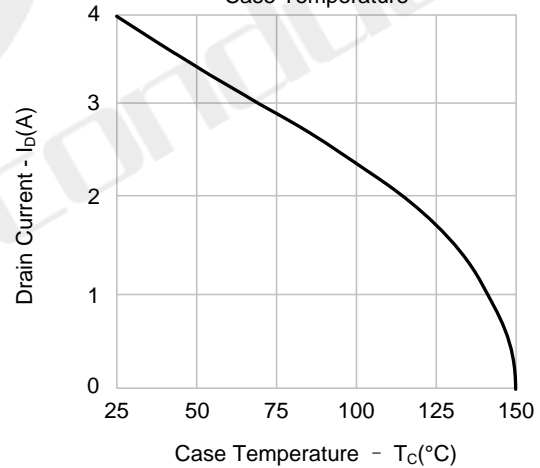
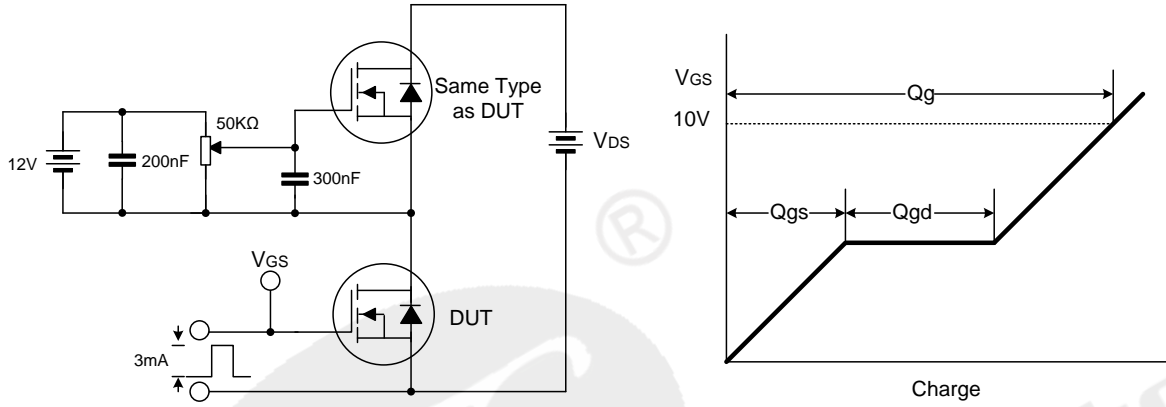


Figure 10. Maximum Drain Current vs. Case Temperature

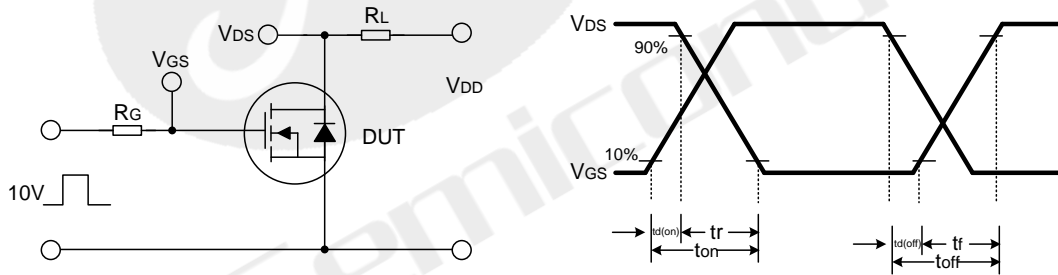


Typical Test Circuit

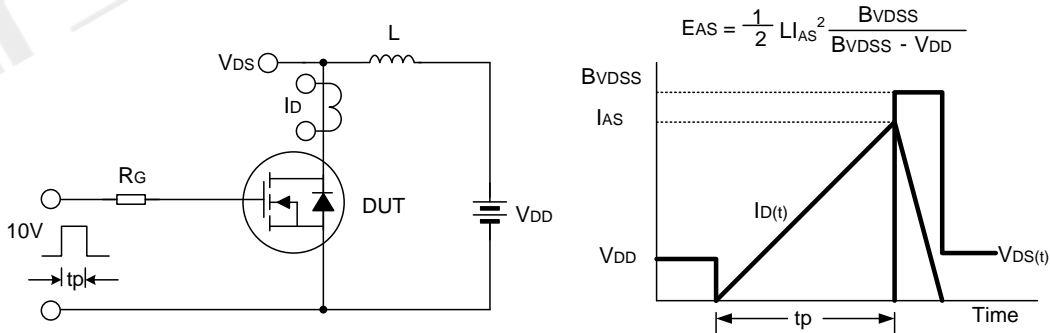
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

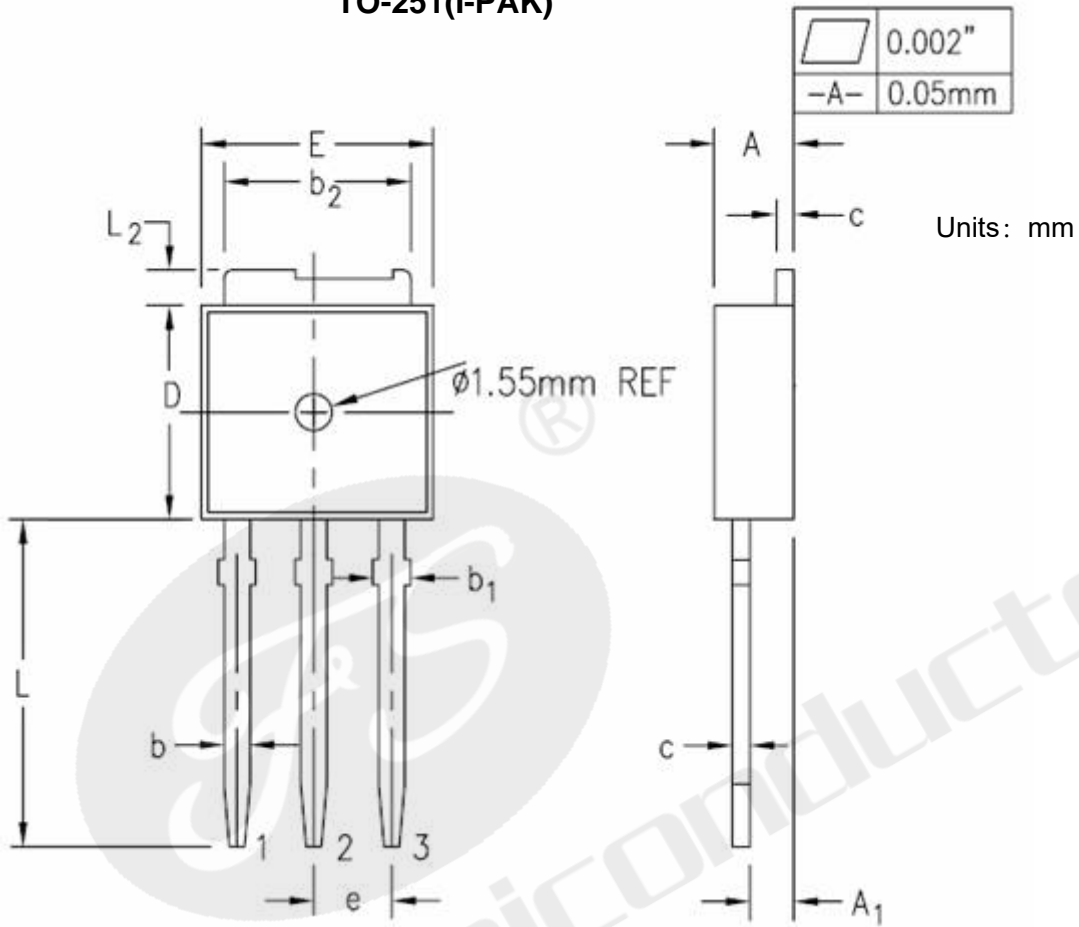


Unclamped Inductive Switching Test Circuit & Waveform



Package Dimensions

TO-251(I-PAK)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	
A1	0.041	0.048	1.04	1.23	
b	0.025	0.035	0.64	0.89	
b1	0.027	0.039	0.69	0.92	
b2	0.206	0.216	5.23	5.48	
c	0.018	0.024	0.46	0.61	
D	0.241	0.249	6.12	6.32	
E	0.250	0.265	6.35	6.73	
e	0.090 TYP.		2.28 TYP.		
L	0.350	0.380	8.89	9.65	
L2	0.035	0.050	0.89	1.27	



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

**ATTACHMENT**

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	

